What is claimed is:

1. A sense amplifier driver which outputs an enable signal for enabling a sense amplifier, the sense amplifier driver comprising:

a first inverter which receives an input signal and outputs an output signal swung between a ground voltage and a control voltage which is determined by the amount of an off-current flowing through at least one transistor in an inactive memory block; and

a second inverter which receives the output signal of the first inverter and delays and buffers the output signal of the first inverter by a period of time inversely proportional to a level of the control voltage.

2. The sense amplifier driver of claim 1, wherein a point in time when the enable signal is activated is varied according to the level of the control voltage.

3. A sense amplifier driver comprising a first inverter and a second inverter, wherein the first inverter comprises:

a first pull-up transistor having a gate for receiving an input signal, a first electrode for receiving a control voltage inversely proportional to the amount of an off-current flowing through at least one transistor in an inactive memory block, and a second electrode connected to an output terminal of the first inverter; and

a first pull-down transistor having a gate for receiving the input signal, a first electrode connected to a ground voltage, and a second electrode connected to the output terminal of the first inverter, and

the second inverter comprises:

a second pull-up transistor having a gate connected to the output terminal of the first inverter, a first electrode connected to a power voltage, and a second electrode connected to an output terminal of the second inverter;

a second pull-down transistor having a gate connected to the output terminal of the first inverter, a first electrode, and a second electrode connected to the output terminal of the second inverter;

a first transistor having a gate connected to the first electrode of the first pull-up transistor of the first inverter, a first electrode connected to the ground voltage, and a

second electrode connected to the first electrode of the second pull-down transistor; and

a capacitor connected between the output terminal of the second inverter and the ground voltage.

4. The sense amplifier driver of claim 3, further comprising at least one of a plurality of second transistors connected between the first electrode of the second pull-down transistor and the second electrode of the first transistor, each transistor of the plurality of second transistors having a gate connected to the first electrode of the first inverter.

5. The sense amplifier driver of claim 4, wherein a sense amplifier enable signal for enabling a sense amplifier is output from the output terminal of the second inverter.

6. A sense amplifier driver comprising N (natural number) inverters connected in a series, wherein an n -1^{th} (n a natural number greater than 2) inverter among the N inverters comprises:

a first pull-up transistor having a gate for receiving an input signal, a first electrode for receiving a control voltage determined by the amount of an off-current flowing through a plurality of transistors, and a second electrode connected to an output terminal of the n-1^{th} inverter; and

a first pull-down transistor having a gate for receiving the input signal, a first electrode connected to a ground voltage, and a second electrode connected to the output terminal of the n-1^{th} inverter, and

an n^{th} inverter among the N inverters comprises:

a second pull-up transistor having a gate connected to the output terminal of the n-1^{th} inverter, a first electrode connected to a power voltage, and a second electrode connected to an output terminal of the n^{th} inverter;

a second pull-down transistor having a gate connected to the output terminal of the n-1th inverter, a first electrode, and a second electrode connected to the output terminal of the nth inverter;

a first transistor having a gate connected to the first electrode of the first pull-up transistor, a first electrode connected to the ground voltage, and a second electrode connected to the first electrode of the second pull-down transistor; and

a capacitor connected between the output terminal of the nth inverter and the ground voltage.

7. The sense amplifier driver of claim 6, wherein an n-2th inverter among the N inverters inverts a clock signal to generate the input signal, and an n+1th inverter among the N inverters is connected to the output terminal of the nth inverter.

8. The sense amplifier driver of claim 6, further comprising at least one of a plurality of second transistors connected between the first electrode of the second pull-down transistor and the second electrode of the first transistor, each transistor of the plurality of second transistors having a gate connected to the first electrode of the n -1th inverter.

9. A memory device comprising:

a memory cell array including a plurality of memory cells;

a delay control signal generation circuit which generates a delay control signal with a voltage determined by the amount of an off-current flowing through at least one transistor;

a sense amplifier driver which receives a clock signal, controls a period of time for which the clock signal is buffered according to the voltage of the delay control signal, and outputs a sense amplifier enable signal; and

a sense amplifier which senses and amplifies data of the memory cell array in response to the sense amplifier enable signal.

10. The memory device of claim 9, wherein the sense amplifier driver includes:

a first inverter which receives the clock signal, and outputs an output signal swung between the voltage determined by the amount of an off-current and a ground voltage; and

a second inverter which receives the output signal of the first inverter, and delays and buffers the output signal of the first inverter by a period of time inversely proportional to a level of the voltage determined by the amount of an off-current.

11. The memory device of claim 9, wherein the period of time for which the clock signal is delayed is inversely proportional to the voltage of the delay control signal.

12. The memory device of claim 9, wherein the sense amplifier driver includes:

a first inverter which converts the clock signal into a signal swung between the voltage inversely proportional to the amount of an off-current and a ground voltage, and outputs the converted signal; and

a second inverter which is connected to the first inverter, controls a period of time for which the output signal of the first inverter is buffered in response to the voltage inversely proportional to the amount of an off-current, and outputs the sense amplifier enable signal,

wherein the period of time for which the output signal of the first inverter is buffered is proportional to the amount of off-current.

13. A memory device comprising:

a memory cell array including a plurality of memory cells;

a delay control signal generation circuit including a dummy bit line and a complementary dummy bit line which are precharged to a predetermined voltage, a plurality of word lines respectively connected to ground voltages, and a plurality of transistors, each transistor having a gate connected to a corresponding word line of the word lines and a first electrode connected to the dummy bit line, a voltage of the dummy

bit line being determined according to a voltage drop due to an off-current flowing through the plurality of transistors;

a sense amplifier driver which receives a clock signal, controls a period of time for which the clock signal is buffered according to the voltage of the dummy bit line, and outputs a sense amplifier enable signal; and

a sense amplifier which senses and amplifies data of the memory cell array in response to the sense amplifier enable signal.

14. The memory device of claim 13, wherein the period of time for which the clock signal is buffered is inversely proportional to the voltage of the dummy bit line.

15. The memory device of claim 13, wherein the sense amplifier driver includes:

a first inverter which receives the clock signal, and outputs an output signal swung between the voltage of the dummy bit line and a ground voltage; and

a second inverter which receives the output signal of the first inverter, and delays and buffers the output signal of the first inverter by a period of time inversely proportional to a level of the voltage of the dummy bit line.

16. A memory device comprising:

a memory cell array including a plurality of memory cells;

a delay control signal generation circuit having a first electrode precharged to a power voltage, and a gate and a second electrode commonly connected to a ground voltage;

a sense amplifier driver which receives a clock signal, controls a period of time for which the clock signal is buffered according to a voltage of the first electrode, and outputs a sense amplifier enable signal; and

a sense amplifier which senses and amplifies data of the memory cell array in response to the sense amplifier enable signal.

17. The memory device of claim 16, wherein the sense amplifier driver includes:

a first inverter which receives the clock signal, and outputs an output signal swung between the voltage of the first electrode and a ground voltage; and

a second inverter which receives the output signal of the first inverter, and delays and buffers the output signal of the first inverter by a period of time inversely proportional to a level of the voltage of the first electrode.

18. A method of outputting an enable signal for enabling a sense amplifier, comprising:

receiving an input signal and outputting an output signal swung between a ground voltage and a control voltage which is inversely proportional to the amount of an off-current flowing through at least one transistor in an inactive memory block; and

receiving the output signal, delaying and buffering the output signal by a period of time inversely proportional to a level of the control voltage, and outputting the enable signal.

19. The method of claim 18, wherein a point of time when the enable signal is activated is varied according to the level of the control voltage.

20. A method of detecting data comprising:

generating a delay control signal with a voltage determined by the amount of an off-current flowing through at least one transistor;

receiving a clock signal, controlling a period of time for which the clock signal is buffered according to the delay control signal, and outputting a sense amplifier enable signal; and

sensing and amplifying data of a memory cell array in response to the sense amplifier enable signal.

21. The method of claim 20, wherein the sense amplifier enable signal generation step includes:

receiving the clock signal and outputting an output signal swung between the voltage determined by the amount of an off-current and a ground voltage; and

receiving the output signal, delaying and buffering the output signal by a period of time inversely proportional to a level of the voltage determined by the amount of an off-current, and outputting the sense amplifier enable signal.